In the Specification:

Please amend the specification as follows:

Amend the paragraph beginning on page 1, line 6 as follows:

This application is a continuation of U.S. Patent Appl No. 10/171,762, which was filed on June 17, 2002, which is a continuation of U.S. Patent Appl No. 09/580,014, which claims the benefit of U.S. Provisional Application No. 60/136,116 filed on May 26, 1999, the contents of all of which [[is]] are hereby incorporated by reference.

Amend the paragraph beginning on page 1, line 9, as follows:

[[This]] The 09/580,014 application is a continuation-in-part of patent application entitled "System and Method for Linearizing a CMOS Differential Pair," by Haideh Khorramabadi, filed May 17, 2000, U.S. Patent Application No. [to be assigned] 09/573,356, (Docket B600:36523); which is a continuation-in-part of Application No. 09/547, 968, filed April 12, 2000; which is a continuation-in-part of Application No. 09/493,942, filed January 28, 2000; which is a continuation-in-part of Application No. 09/483,551, filed January 14, 2000; which is a continuation-in-part of Application No. 09/439,101 filed November 12, 1999; the disclosures of which are incorporated herein by reference.

Amend the paragraph beginning on page 105, line 8, as follows:

The details of linearizing a CMOS differential pair are disclosed in more detail in U.S. Patent Application No. 09/573,356, filed May 17, 2000, (B600:36523) entitled "System and Method for Linearizing a CMOS Differential Pair" by Haideh Khorramabadi; based on U.S. Provisional Application No. 60/136,115 filed May 26, 1999 (B600:34678), the subject of which is incorporated in this application in its entirety by reference.

Amend the paragraph beginning on page 105, line 27, as follows:

The details of Q enhanced filters are disclosed in more detail in U.S. Patent Application No. [[_____]] 09/573,356, filed May 17, 2000(B600: 36523) entitled, "System and Method for Linearizing a CMOS Differential Pair" by Haideh Khorramabadi; based on U.S. Provisional Application No. 60/136,115 filed May 26, 1999 (B600:34678), the subject matter of which is incorporated in this application in its entirety by reference. Once an improved Q is achieved it is desirable to maintain it over the range of temperatures encountered in a circuit operation with temperature compensation circuitry 3206.

Amend the paragraph beginning on page 126, line 32 as follows:

The indirect synthesis of the first and second LOs utilizes a frequency reference generated by a 10 MHz crystal oscillator 4508 [[5408]]. The 10 MHz crystal oscillator utilizes the previously disclosed differential signal transmission and a unique design that advantageously tends to provide an extremely low phase noise reference signal.

Amend the paragraph beginning on page 129, line 25 as follows:

FIG. 45d is a block diagram of an embodiment of a VCO having a tuning control circuit and showing tuning control circuit interaction with major VCO components. A typical VCO as known to those skilled in the art comprises circuitry that implements the subsystems shown in FIG. 45d. Typical VCO subsystems comprise a gain block 4599, a feedback network 4505 and a summing junction 4507 that couples the amplifier output, as modified by the feedback network, to the amplifier input. These functions are often implemented by circuit components that possess [[poses]] interconnections that are not as easily identifiable as shown. However, in any functioning oscillator the functional subsystem and interconnections as illustrated are present.

Amend the paragraph beginning on page 130, line 5 as follows (commas added for readability):

A VCO is an oscillator that produces a variable frequency output f_{out}, that is proportional to a control voltage input 4533. A VCO is typically integrated on an integrated circuit substrate 4503. Major VCO components of a VCO comprise an amplifier 4599, a source of feedback, such as feedback network 4505 typically comprising a resonant tank circuit, and a path to couple the feedback to the amplifier's input represented by a summing junction 4507.

Amend the paragraph beginning on page 131, line 5 as follows:

FIG. 45e is a schematic of the feedback network 4505 that allows the frequency of oscillation to be adjusted. The feedback network comprises capacitive 4511 and inductive 4509 circuit elements having frequency dependent responses. The feedback network typically comprises multiple circuit elements to produce an overall frequency response. Equivalently the feedback network is intertwined with the amplifier circuit (or gain stage) (4599 of FIG. 45d). For example, a feedback network comprising an LC tank circuit as shown in FIG. 45e [[44e]] will resonate at a frequency dependent upon the combined values of inductance 4509 and capacitance 4511. If a variable capacitance 4515 is included, as shown in FIG. 45f, a resonant frequency may be tuned over a range of frequencies by adjusting the capacitance 4515. Alternatively, an inductor 4509 may be of the variable type to adjust the output frequency 1904. However, an adjustable capacitance 4511 is typically easier to fabricate on an integrated circuit substrate than a tuned inductor 4509.

Amend the paragraph beginning on page 131, line 22 as follows:

FIG. 45f is a schematic of a feedback network that allows the frequency of oscillation to be adjusted continuously by varactor tuning. Varactors typically provide a fine tuning range of adjustment in a VCO. In an embodiment, a continuously adjustable capacitance is provided by

varactor diodes 4515. A varactor diode is a diode that possesses [[poses]] a varying amount of capacitance. The amount of capacitance depends [depending] upon a level of direct current biasing the varactor diode. To set the varactor's tuning range, a fixed capacitance 4513 is typically used. The fixed capacitor typically gets the tuned circuit close to a desired frequency, and the varactor fine tunes the desired frequency. In an alternate embodiment, a network of discretely [discreetly] switched capacitors may be used in place of fixed capacitor 4513. In the later described arrangement utilizing discretely [[discreetly]] switched capacitors, discrete ranges of tunable frequencies, with each range being continuously tunable, are [[is]] provided.

Amend the paragraph beginning on page 133, line 15 as follows:

FIG. 45g is a graph of capacitance versus [[verses]] control voltage applied to an NMOS varactor. As can be seen from this graph, varactor capacitance 4511 tends to be inversely proportional to an applied control voltage 4533. A portion of the curve tends to be linear 4521. It is desirable to utilize the linear portion of the tuning curve to tune the VCO. Such a curve is often referred to as a C-V curve.

Amend the paragraph beginning on page 133, line 25 as follows:

Equivalent series resistance or ESR is a figure of merit for a capacitor. The ESR of an NMOS varactor is the drain source resistance of the shortened leads. In an exemplary design, the NMOS FETs used to form the varactors have [[an atomic]] a W/L ratio equal[[s]] to (20.0/0/35) that is repeated 36 times.

Amend the paragraph beginning on page 135, line 15 as follows:

The amplifier circuit 4599 consists of a pair of NMOS driver transistors M1 M2. The NMOS drivers each possess [[poses]] an inherent capacitance C_{gs} that tends to contribute to the tuning of the VCO.

Amend the paragraph beginning on page 135, line 29 as follows:

Transistor M2 has its source coupled to ground. The drain of M2 is coupled to the gate [[base]] of M1, a first terminal of a second inductor 4509, the first terminal of a second veractor 4515 and a set of first terminals of a second bank of six capacitors 4528. A set of second terminals of the second bank of six capacitors are each coupled to one of a second set of six transistor switches 4527 drains. The sources of the second set of switching transistors are coupled to ground. The gates of each of the switching transistors are coupled to individual control lines b_1 through b_n 4520 that emanate from the tuning control circuit (4535 of FIG. 45d).

Amend the paragraph beginning on page 136, line 12 as follows:

The adaptive [[Adaptive]] bias circuit 4522 comprises a PMOS transistor M3 with its drain coupled to a voltage supply V_{DD} and a first terminal of a capacitor 4531. The second terminal of capacitor 4531 is coupled to the gate of M3. The gate of M3 is also coupled to the first terminal of a resistor 4524. The second terminal of resistor 4524 is coupled to the adaptive bias control line 4530 that is supplied by a constant G_m bias cell 4536.

Amend the paragraph beginning on page 137, line 20 as follows:

FIG. 45j is a schematic of an equivalent circuit model of the VCO of FIG. 45i. In an embodiment, a design provides specific phase noise performance. The noise contribution [[contributions]] is primarily due to flicker noise of the transistors, varactors, and the bias circuit.

Amend the paragraph beginning on page 137, line 25 as follows:

In modeling an equivalent circuit, as long as the tunable [[tuneable]] capacitance is a small fraction of the fixed tank capacitance, the flicker noise ("1/f") contribution of the varactors is minimal.

Amend the paragraph beginning on page 137, line 28 as follows:

Up-conversion of 1/f noise is minimized by maximizing the gate threshold voltage ("V_{gt}") of M1 and M2 of FIG. 45i [[45j]], and making the transistors reasonably large. In making the transistors large the total gate capacitance present in the circuit is a constraint. The biasing transistor M3 of FIG. 45i [[44j]] is made wide and short to maximize gate area and minimize its head room impact. Headroom impact refers to the fact that to reduce power consumption the inductors 4509 are not coupled directly to V_{DD}. As the W/L ratio of M3 is reduced, a larger voltage is dropped across the drain and source terminals of M3. To provide sufficient headroom in the described embodiment it is desired to maintain $V_{DS} > (V_{SG} - V_t)$. In a final effort to reduce 1/f noise, the gate of transistor M3 of FIG. 45i [[44j]] is filtered by a 100k OHM on-chip resistor 4524 and a 0.1 μF external capacitor 4531, both of FIG. 45i [[45j]]. The filtering ensures that noise from the small bias devices does not adversely affect the overall noise performance of the VCO core shown in FIG. 45i [[44j]]. The low pass filter possesses a 10ms time constant that does not affect startup as the external 0.1 [[.1]] μF capacitor is initially charged through a switch having a worse case on-resistance of substantially 50 OHMS. The 0.1 [[.1]] μF capacitor and 50 OHM resistance provide an acceptable time constant for circuit performance.

Amend the paragraph beginning on page 138, line 17 as follows:

The small signal circuit model shown in FIG. 45j [[45k]] is a reasonable approximation of the VCO since the switched capacitors and varactors are designed to have a Q that is much

greater than the inductors. Thermal noise arising from the substrate and gate resistance is minimized through careful design and layout techniques known to those skilled in the art. The equivalent parallel resistance of the tank is 2R, where R is approximately equal to $(Q^2)r$.

Amend the paragraph beginning on page 138, line 25 as follows:

FIG. 45k is a schematic of a tuning control circuit controlling switched capacitors tending to center a varactor tuning range. In FIG. 45k, [[441]] variable capacitors 4511 of FIG. 45f [[44f]] are [[is]] represented by a single fixed capacitor 4513, ~~4509 and~~ a series of switched capacitors C_1 4528 through C_n 4528, and a continuously variable capacitance provided by a pair of varactors 4515. The capacitors utilized in the circuit may be of any type including those suitable for integrated circuit fabrication. In an embodiment, metal fringe capacitors are used for the switched capacitors. The parallel combination of the capacitors provides the required overall capacitance C as shown in FIG. 45e [[44f]]. In alternative embodiments, capacitance in the tuned circuit may be made up of any number or combination of fixed capacitors and switched capacitors. Capacitors C_1 through C_n are discrete capacitors that are added or removed from the tuned circuit by a field effect transistor ("FET") switch.

Amend the paragraph beginning on page 139, line 8 as follows:

Each switch is activated through an individual control line that is part of a bus of control signals 4520 emanating from the tuning control circuit 4535. In alternative embodiments, the number of control lines may be reduced to less than one per switch by addressing a demultiplexer through [[a]] one or more multiplexed lines. The presence of a voltage on any one of the given control lines, sufficient to turn on the channel of the field effect transistor, effectively couples the capacitors 4528 to the tunable resonance circuit 4505.

Amend the paragraph beginning on page 139, line 25 as follows:

The tuning control circuit makes use of a temperature and process dependent moving window of acceptable control voltages defined by a range of voltages that vary with temperature and process. The moving window tends to aid in optimally choosing a range of valid control voltages for the PLL that tend to aid in attaining a frequency lock. The control circuit uses the moving window to center a varactor diode's (4515 [[4415]] of FIG. 45k) tuning range by adding or removing capacitance. Centering tends to avoid gross varactor non-linearities by causing a range of control voltage being utilized to fall on a linear operating region of a C-V curve. Also, the circuit tends to mitigate dead band conditions and tends to improve loop stability over process and temperature conditions.

Amend the paragraph beginning on page 141, line 11 as follows:

Returning to FIG. 46a, the phases of the two phase detector inputs 4612, 4616 are compared in the phase detector 4614. A pulse train representing the phase difference is output 4620 from the phase detector and coupled to the input of a charge pump 4622. The charge pump is conventionally constructed as is known by those skilled in the art. The output of the charge pump is fed into a low pass filter 4624. The output of the low pass filter 4624 is fed into the control voltage input of the VCO 4532 [[4618]]. The VCO outputs an image and quadrature signal 1904 at a frequency as set by the frequency select line 4608.

Amend the paragraph beginning on page 142, line 5 as follows:

Voltages V1 and V2 are taken from a resistive divider circuit that utilizes a transistor to track process and temperature variations. A conventional voltage reference 4607 outputting voltage at level V1 is applied to a first terminal of a first resistor 4603 and the negative input of msb comparator 4636. A second terminal of the first resistor is coupled to a first terminal of a

second resistor 4605 at node 4637. A second terminal of the second resistor 4605 defining [[defines]] voltage threshold V2 is coupled to a drain of a transistor M4. The drain of M4 is coupled to the negative terminal of lsb comparator 4634. A source of M4 is coupled to ground, and a gate of M4 is coupled to node 4637.

Amend the paragraph beginning on page 142, line 17 as follows:

Comparator 4634 outputs signal lsb and comparator 4636 output signal msb. Voltages V1 and V2 set thresholds to form a sliding window which monitors the state of the closed PLL by monitoring voltage 4510 at low pass filter 4624. Control voltage 4510 is taken as the voltage across a capacitor 4613 in the low pass filter that induces a zero in the loop filter 4624. Thus, the control voltage is a filtered version of the control voltage of the PLL loop, and thus tends to have eliminated spurious components present on the VCO control line.

Amend the paragraph beginning on page 142, line 34 as follows:

The reset signal 4512 is based on the output of low pass filter ("LPF") 4624 and is applied to the VCO control circuit as described below. The reset signal 4512 is generated external to the circuit depicted in FIG. 46a and is an input to this circuit as shown in FIG. 46a. Low pass filter 4624 takes its input from charge pump 4622's output. A first shunt capacitor 4609 has a first terminal coupled to the LPF input and it has a second terminal that is shunted to ground. Resistor 4611 has a first terminal coupled to the LPF input and a second terminal coupled to the first terminal of a capacitor 4613. A second terminal of capacitor 4613 is coupled to ground, a drain coupled to the first terminal of capacitor 4613, and a gate that receives [[defines]] a reset signal 4512 utilized throughout the VCO control circuit. The reset signal is coupled to an R terminal

of DQ flip-flop 4644, a reset terminal "R" of the 6-bit bi-directional tuning register 4630, the "R" input of DQ flip-flop 4617, and a first input of a two input OR gate 4619.

Amend the paragraph beginning on page 143, line 17 as follows:

Clock signal 4514 is based on the divided reference oscillator signal 4612. Division of the reference signal is accomplished in any conventional manner, known by those skilled in the art. Clock signal 4514 is coupled to the clock inputs of DQ flip-flops 4644 and 4617, a clock input of the 6-bit [6-bot] bi-directional tuning register 4630, and in-lock detector 4648. The clock signal is also applied to an inverted second input of the two input AND [[and]] gate 4646.

Amend the paragraph beginning on page 143, line 33 as follows:

For example, for a change in temperature, the V_{gs} of M1 and M2 would change. A change in the V_{gs} of M1 and M2 causes the capacitance of the varactor to change. If a window that did not track the change of V_{gs} was not provided, then at elevated temperature the loop would not lock. At start-up, when the chip is at room temperature, V1 is set to 1.5 volts and V2 is set to 1.0 volt. The phase lock loop will attempt to lock with a voltage between 1.0 and 1.5 volts. Over time, the chip temperature increases causing the V_{gs} of M1 and M2 to change. The capacitance changes in the varactor cause [[causes]] the VCO to move away from the preset window. If the PLL tried to acquire lock at the elevated temperature, it would not be able to do so within a voltage range of 1.0 to 1.5 volts.

Amend the paragraph beginning on page 145, line 3 as follows:

Returning to block 4702, if the control voltage is out of range, a decision is made 4706 based on[,] whether [[wether]] the control voltage is above or below the desired range. If the

control voltage is greater than the control voltage range, a capacitance is removed from the VCO circuit 4708. The process flow is routed to the beginning of the process, where the control voltage is again reevaluated 4702.

Amend the paragraph beginning on page 145, line 14 as follows:

The VCO tuning control circuitry 4535 [[4604]] of FIG. 46a functions to carry out the process of FIG. 47a. If the voltage of the loop lies outside the window defined by the threshold voltages V1 and V2, [.] the [[The]] clock input to the 6-bit bi-directional tuning register 4630 is enabled. This register function may be provided by a conventional circuitry known in the art to provide this function and is not limited to the circuitry depicted. A "lock time out" circuit 4648 of FIG. 46a is reset on the rising edge of the clock signal to the 6-bit bi-directional tuning register 4630 of FIG. 46a. The "lock time out" circuit is conventionally constructed and is not limited to the components depicted in FIG. 46a.

Amend the paragraph beginning on page 145, line 26 as follows:

If control voltage 4510 [[4632]] exceeds the upper threshold set by the comparators, zeros are shifted through the register 4630. A zero voltage decreases the capacitance in the VCO tuning circuitry by switching out a capacitance controlled by one of the 6 control lines 4520 [4628]. Alternatively, any suitable number of control lines may be used other than [[then]] the exemplary six. This shifting of values in a register allows one of six exemplary capacitor switch control lines to be activated or deactivated, an evaluation made and another line activated or deactivated so that the previous tuning setting is not lost. This function may be implemented by passing a value (on or off) down a line of capacitors by shifting or by activating a capacitor associated with a given line and then a next capacitor without shifting the capacitance control signal.

Amend the paragraph beginning on page 146, line 7 as follows:

If the control voltage 4510 [[4632]] is less than the lower threshold voltage of the comparator 4634, ones are shifted through the 6-bit bi-directional tuning register. The ones increase the capacitance applied in the VCO tuning circuit by switching in a capacitance controlled by one of the 6 control lines 4520 [[4628]].

Amend the paragraph beginning on page 146, line 12 as follows:

Once control voltage 4510 [[4632]] enters the predetermined valid range of operation as set by voltages V1 and V2, the shift register 4630 is disabled. At this time, the locked time out circuit 4648 is enabled. If the lock time out circuit remains enabled for the predetermined time period, that satisfies the in lock condition for the PLL, and the clock to the DQ flip-flop 4644 is disabled, thus disengaging the control circuit. The functions described in this paragraph are constructed from standard logic components known to those skilled in the art, and are not limited to those components depicted in FIG. 46a.

Amend the paragraph beginning on page 146, line 34 as follows:

After initiation of the process, the logic circuits are reset 4703. Logic signals to be reset comprise a state signal 4510, and a reset signal 4512 that are inputs to the tuning control circuit 4535, as shown in FIG. 46a.

Amend the paragraph beginning on page 147, line 5 as follows:

The next process step is directed to setting an initial VCO oscillator frequency. A tuning register 4630 (of FIG. 46a) is set to produce an output of all ones at process step 4705. An output of all ones causes all capacitors in the VCO to be switched into a feedback network circuit 4505 through control lines 4520 (shown in FIG. 45k). With [[with]] a maximum value of capacitance

switched into the feedback network, the VCO is tuned to its lowest frequency where the frequency F is given by the relation,

$$F = 1/(2\pi\sqrt{LC}) \qquad (7.25)$$

F = frequency in Hz (hertz)

L = inductance in H (henry)

C = capacitance in F (farad)

Next, the zero cap in a loop filter 4624 [[5524]](of FIG. 46a) is zeroed in the next process step 4707.

Amend the paragraph beginning on page 147, line 24 as follows:

The tuning control circuit 4535 has now been initialized and VCO tuning 4709 is commenced. To tune the VCO, an MSB and an LSB signal are sampled every 64th clock cycle 4711 in an embodiment. The MSB signal is the output of comparator 4636 of FIG. 46a. The LSB signal is the output of a comparator 4634 also shown in FIG. 46a [46]. The action taken in tuning the PLL depends upon the state of the MSB and LSB signals. First, an evaluation is made to determine if the MSB and LSB signals are both equal to one 4713. If the signals are both in the ones state, a capacitor is switched into the circuit 4720. The state of the circuit continues to be monitored [[monitors]] and if the MSB and LSB are not equal to one, a further evaluation is made. Next, the MSB and LSB are evaluated to determine if both signals are equal to a zero value 4716. If both signals are equal to the zero state, a switched capacitor is removed 4722. The signal continues to be monitored every 64th clock cycle 4711 and when the MSB and LSB signals are not both equal to one or zero, a determination is made as to whether the MSB signal is equal to zero and the LSB signal is equal to one [[zero]] 4718. If the signal does not meet this condition, the signal continues to be monitored with the capacitance adjusted until the

MSB is equal to zero and the LSB is equal to one for three clock cycles. Once this condition has been met, the PLL is deemed to be in lock 4724. The circuit condition continues to be monitored and if the PLL remains in lock for 15 reference clock cycles, the tuning circuit is disabled 4726, and the process is ended 4728.

Amend the paragraph beginning on page 148, line 17 as follows:

FIG. 47c is a graph of a family of frequency versus [[verses]] control voltage for various capacitor values that illustrates the use of comparator hysteresis to aid in achieving a frequency lock condition. The first embodiment of the invention does not utilize hysteresis. An [[an]] alternative embodiment of the invention utilizes hysteresis. Comparators 4636 [[4656]], 4634 of FIG. 46a are shown as having hystersis incorporated in their design. Returning to FIG. 47c, the comparator's hysteresis about a voltage level V_L is shown by range Δ 4730. In an embodiment, hysteresis is employed to help achieve a PLL lock condition 4732 corresponding to a frequency F_1 at control voltage level V_L corresponding to a tuning capacitance value C_2.

Amend the paragraph beginning on page 149, line 15 as follows:

FIG. 47d is a graph of a family of frequency versus [[verses]] control voltage for various capacitor values that illustrates the use of dual comparator windows to aid in achieving a frequency lock condition. The graph illustrates the sliding window of valid lock ranges provided by the design. A valid lock range for a low V_{GT} and a high V_{GT} are shown. The voltage range of the window is constant. However, the starting and ending values of the window vary.

Amend the paragraph beginning on page 149, line 23 as follows: